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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,628	07/21/2003	Luan C. Tran	MI22-2356	6591

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,628	LUAN C. TRAN	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *45-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *45-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/15/05, 5/16/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 45, 48 and 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Yuan et al. (U.S. Patent No. 5,534,456).

In re claim 45, Yuan et al. disclose a method of forming a semiconductor construction, comprising:

forming a layer of patternable material (79) over a semiconductive substrate material (31);

patterning the layer of patternable material to form at least two patterned blocks, a pair of adjacent blocks being separated by a first gap (see column 9, lines 1-6 and Figures 8A-C);

forming a coating (87) over the pair of adjacent blocks and across the first gap between the adjacent blocks;

selectively removing the coating from across the first gap while leaving the coating along sidewalls and elevationally over the pair of adjacent blocks (spacers 89 and 91 extend along sidewalls and elevationally over 79); the pair of blocks and coating together defining a pair of enlarged blocks that are separated by a second gap; the second gap being narrower than the first gap (see (b)

while the enlarged blocks remain over the semiconductive substrate material, implanting at least one dopant within the semiconductive material within the second gap to form a doped region (see column 9, lines 25-60); and

removing the enlarged blocks from over the semiconductive substrate material (see Figure 10A-C and column 9, line 60 through column 10, line 65).

In re claim 48, Yuan et al. disclose the method wherein the patterned blocks are formed by a photolithographic process, wherein the photolithographic process is limited to a minimum feature size that can be obtained by the photolithographic process, the first gap corresponding to about the minimum feature size; and wherein the doped region of the semiconductive material formed by the implanting has a region width that is less than the minimum feature size (see column 9, lines 1-7 and 25-40).

In re claim 49, the method wherein the region width is less than or equal to about 50% of the minimum feature size (see column 9, lines 25-40.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 45 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. Patent No. 6,750,150) in view of Yu et al. (U.S. Patent No. 6,180,468).

In re claim 45, Chung et al. disclose a method of forming a semiconductor construction, comprising:

forming a layer of patternable material (130) over a semiconductive substrate material;

patterning the layer of patternable material to form at least two patterned blocks, a pair of adjacent blocks being separated by a first gap (see column 3 lines 5-20);

forming a coating (150) over the pair of adjacent blocks and across the first gap between the adjacent blocks;

selectively removing the coating from across the first gap while leaving the coating on the pair of adjacent blocks; the pair of blocks and coating together defining a pair of enlarged blocks that are separated by a second gap; the second gap being narrower than the first gap (see Figure 3A).

Chung et al. does not disclose the method of while the enlarged blocks remain over the semiconductive substrate material, implanting at least one dopant within the semiconductive substrate material within the second gap to form a doped region and removing the enlarged blocks from over the semiconductive substrate material.

Yu et al. discloses the method of while the enlarged blocks remain over the semiconductive substrate material, implanting at least one dopant within the semiconductive material within the second gap to form a doped region (see Figure 4

and column 4, lines 28-33); and removing the enlarged blocks (see Figure 5 and column 4, lines 28-33) from over the semiconductive substrate material

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implant through the narrowed blocks of Chung et al. in order to form a sublithographic feature allowing for devices per area during further semiconductor processing, and because as Yu et al. discloses implanting through the narrowed gap prevents parasitic capacitance. The examiner notes that Chung et al. method of sublithographic processing is a general teaching could be applied to any method of making sublithographic devices.

In re claim 50, Yu et al. disclose the method further comprising: forming a first source/drain region and a second source/drain region (14, 16) within the semiconductive substrate material, the first source/drain region being laterally spaced from a first edge of the doped region and the second source/drain region being laterally spaced from a second opposing edge of the doped region (see Figure 6); and forming an isolation mass (48) over the doped region, the first and second source/drain regions extending partially under the isolation mass.

Claims 46 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. Patent No. 6,750,150) and Yu et al. (U.S. Patent No. 6,180,468) in view of DeJule (Cahners Semiconductor International Website, "Paths to Smaller Features" provided in IDS 11/13/03) .

In re claim 46, Chung e t al. and Yu et al. disclose the method as claimed and rejected above including the method of forming a patternable material of photoresist (130, Chung et al.).

Chung et al. does not disclose the method wherein the coating comprises a material which cross-links when exposed to the acid from the photoresist and wherein the coating corresponds to a material designated as AZ R200™ by Clariant International, Ltd.

DeJule discloses the method of utilizing a coating comprising a material which cross-links when exposed to the acid from the photoresist and wherein the coating corresponds to a material designated as AZ R200™ by Clariant International, Ltd. (see entire page).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the coating of DeJule in the method Chung et al. and Yu et al. because as DeJule teaches that the method utilizing AZ R200™ by Clariant International, Ltd allows for sublithographic dimensions as required in the Yuan et al. reference, while minimizing costs.

Claims 45 and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamatsu et al. (U.S. Patent No. 5,440,161) in view of Chung et al. (U.S. Patent No. 6,750,150) and Yu et al. (U.S. Patent No. 6,180,468)

Iwamatsu et al. disclose the method of forming isolation gates (15, 16, 17) including the method of forming a first source/drain region (7,8) and a second

source/drain region (7,8) within the semiconductive substrate material, wherein the isolation mass comprises a gate stack (16, 17), the gate stack comprising a layer of conductively doped material separated from the doped region by an insulative material layer (15), the layer of conductively doped material being majority doped with a p-type dopant, and wherein the source/drain regions are majority doped with an n-type dopant (see column 18, lines 20-35), and the method further comprising forming a pair of transistor devices over the semiconductor substrate, the transistor devices being electrically isolated from one another by the isolation mass (see Figure 1).

Iwamatsu et al. does not disclose the method of forming the doped channel region of the isolation gate including forming a layer of patternable material over a semiconductive substrate material, patterning the layer of patternable material to form at least two patterned blocks, a pair of adjacent blocks being separated by a first gap, forming a coating over the pair of adjacent blocks and across the first gap between the adjacent blocks, selectively removing the coating from across the first gap while leaving the coating on the pair of adjacent blocks; the pair of blocks and coating together defining a pair of enlarged blocks that are separated by a second gap; the second gap being narrower than the first gap, while the enlarged blocks remain over the semiconductive substrate material, implanting at least one dopant within the semiconductive material within the second gap to form a doped region and removing the enlarged blocks from over the semiconductive substrate material.

Chung et al. disclose a method of forming a semiconductor construction, comprising:

forming a layer of patternable material (130) over a semiconductive substrate material;

patterning the layer of patternable material to form at least two patterned blocks, a pair of adjacent blocks being separated by a first gap (see column 3 lines 5-20);

forming a coating (150) over the pair of adjacent blocks and across the first gap between the adjacent blocks;

selectively removing the coating from across the first gap while leaving the coating on the pair of adjacent blocks; the pair of blocks and coating together defining a pair of enlarged blocks that are separated by a second gap; the second gap being narrower than the first gap (see Figure 3A).

Chung et al. does not disclose the method of while the enlarged blocks remain over the semiconductive substrate material, implanting at least one dopant within the semiconductive substrate material within the second gap to form a doped region and removing the enlarged blocks from over the semiconductive substrate material.

Yu et al. discloses the method of while the enlarged blocks remain over the semiconductive substrate material, implanting at least one dopant within the semiconductive material within the second gap to form a doped region (see Figure 4 and column 4, lines 28-33); and removing the enlarged blocks (see Figure 5 and column 4, lines 28-33) from over the semiconductive substrate material

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped region of Iwamatsu et al. by the combined method of Chung and Yu by implanting through the narrowed blocks of Chung et al. as

Yu et al. does in order to form a sublithographic feature allowing for devices per area during further semiconductor processing, and because as Yu et al. discloses implanting through the narrowed gap prevents parasitic capacitance. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the narrowed blocks by the method of Chung et al. because the method allows for sublithography while protecting the patterned layer. The examiner notes that Chung et al. method of sublithographic processing is a general teaching could be applied to any method of making sublithographic devices.

Response to Arguments

Applicant's arguments with respect to claims 45-52 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk